Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An integrated circuit comprising:

a lower metal interconnect layer located over a semiconductor body;

a multi-level dielectric layer located over said lower interconnect layer;

an upper metal interconnect layer located over said multi-level dielectric layer; ~~and~~

a thin film resistor embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer;

a first via extending from said upper metal interconnect layer to said lower interconnect layer; and

a second via extending from said upper metal layer to said thin film resistor.

Claim 2 (cancelled)

Claim 3 (original): The integrated circuit of claim 1, wherein said thin film resistor comprises a hard mask located over an end of the thin film resistor.

Claims 4-5 (cancelled).

Claim 6 (original): The integrated circuit of claim 1, wherein said thin film resistor comprises TaN.

Claim 7 (original): The integrated circuit of claim 1, wherein said thin film resistor comprises SiCr.

Claim 8 (original): The integrated circuit of claim 1, wherein said thin film resistor comprises NiCr.

Claims 9-20 (cancelled)

Claim 21 (previously presented): An integrated circuit comprising:

a lower metal interconnect layer located over a semiconductor body;

a multi-level dielectric layer located over said lower interconnect layer;

an upper metal interconnect layer located over said multi-level dielectric layer; and

a thin film resistor embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer, wherein said thin film resistor comprises a hard mask located over an end of the thin film resistor, and wherein said hard mask comprises TiW.

Claim 22 (previously presented): An integrated circuit comprising:

a lower metal interconnect layer located over a semiconductor body;

a multi-level dielectric layer located over said lower interconnect layer;

an upper metal interconnect layer located over said multi-level dielectric layer; and

a thin film resistor embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer, wherein said thin film resistor comprises a hard mask located over an end of the thin film resistor, and wherein said hard mask comprises TiN.